

What is claimed is:

sub
AI

1 1. A semiconductor device, comprising:
2 a plurality of metal line patterns having a predetermined surface area
3 size, wherein two adjacent metal line patterns are spaced apart from each
4 other at a predetermined distance.

1 2. A semiconductor device as claimed in claim 1, wherein the
2 predetermined distance is greater than 1.0 μm .

1 3. A semiconductor device as claimed in claim 1, wherein the
2 predetermined distance is greater than 1.5 μm .

1 4. A semiconductor device as claimed in claim 1, wherein the
2 plurality of metal line patterns have a surface area size of greater than
3 "30 μm ×30 μm ".

1 5. A semiconductor device, comprising:
2 a metal line layer having a plurality of metal line patterns spaced apart
3 from each other; and
4 at least one underlying layer under the metal line layer,
5 wherein the space between two adjacent metal line patterns has a
6 sufficient width to prevent a crack from occurring in the underlying layer.

1 sub
Ar > 6. A semiconductor device as claimed in claim 5, wherein the
2 width of the space is greater than 1.0 μm .
cont'd

1 7. A semiconductor device as claimed in claim 5, wherein the
2 width of the space is greater than 1.5 μm .

1 8. A semiconductor device as claimed in claim 5, wherein the
2 underlying layer is an insulating layer.

1 9. A semiconductor device as claimed in claim 5, wherein the
2 metal line pattern has a surface area size of greater than "30 μm ×30 μm ".

1 10. A semiconductor device, comprising:
2 a plurality of metal line patterns, wherein two adjacent metal line
3 patterns are spaced apart from each other, and at least one of the two
4 adjacent metal line patterns has a slit.

1 11. A semiconductor device as claimed in claim 10, wherein the slit
2 has a width of greater than 1.0 μm .

1 12. A semiconductor device as claimed in claim 11, wherein the slit
2 is formed at a predetermined distance from an edge of the metal line pattern.

1 3. A semiconductor device as claimed in claim 12, wherein the
2 predetermined distance is less than 4 μm .

1 14. A semiconductor device having a multi-layered structure,
2 comprising:
3 a metal line layer having a plurality of metal line patterns spaced apart
4 from each other;
5 at least one underlying layer under the metal line layer; and
6 a slit formed at a sufficient distance from a space between two
7 adjacent metal line patterns to prevent a crack from occurring in the
8 underlying layer.

1 15. A semiconductor device as claimed in claim 14, wherein the slit
2 is formed in a direction parallel to the space between two adjacent metal line
3 patterns.

1 16. A semiconductor device as claimed in claim 14, wherein the slit
2 has a width greater than 1.0 μm .

1 17. A semiconductor device as claimed in claim 14, wherein the
2 distance from the space between the two adjacent metal line patterns to the
3 slit is less than 4.0 μm .

1 ^{sub} A > 18. A method of manufacturing a semiconductor device having a
2 multi-layered structure, comprising:
3 forming at least one underlying layer on a semiconductor substrate;
4 and
5 forming a metal line layer on the underlying layer, the metal line layer
6 having a plurality of metal line patterns spaced apart from each other at a
7 predetermined distance.

1 19. A method as claimed in claim 18, wherein the predetermined
2 distance is greater than 1.0 μm .

1 20. A method as claimed in claim 18, wherein the predetermined
2 distance is greater than 1.5 μm .

1 21. A method of manufacturing a semiconductor device having a
2 multi-layered structure, comprising:
3 forming at least one underlying layer on a substrate;
4 forming simultaneously a metal line layer on the underlying layer and
5 a slit, the metal line layer having a plurality of metal line patterns spaced
6 apart from each other, at least one of either of two adjacent metal lines has a
7 slit.

1 22. A method as claimed in claim 21, wherein the slit is formed in a
2 direction parallel to the space between two adjacent metal line patterns.

سید
A
کرم

1 23. A method as claimed in claim 21, wherein a width of the slit is
2 greater than 1.0 μm .

1 24. A method as claimed in claim 21, wherein a distance from the
2 space between two adjacent metal line patterns to the slit is less than
3 4.0 μm .

1 25. A method of manufacturing a semiconductor device,
2 comprising:
3 forming at least one underlying layer on a substrate;
4 forming simultaneously a metal line layer on the underlying layer and
5 a slit, the metal line layer having a plurality of metal line patterns spaced
6 apart from each other, the slit formed at a sufficient distance from a space
7 between the two adjacent metal line patterns in order to prevent a crack from
8 occurring in the underlying layer.

1 26. A method as claimed in claim 25, wherein the slit is formed in a
2 direction parallel to the space between two adjacent metal line patterns.

1 27. A method as claimed in claim 25, wherein the width of the slit
2 is greater than 1.0 μm .

1
2
3

sub
A
cont

28. A method as claimed in claim 25, wherein the distance
between the slit and the space between two adjacent metal line patterns is
less than 4.0 μm .

2025-03-27 14:00:00